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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/933,492	08/20/2001	David R. Hembree	00-0625.1	6973

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STEPHEN A GRATTON
THE LAW OFFICE OF STEVE GRATTON
2764 SOUTH BRAUN WAY
LAKEWOOD, CO 80228

EXAMINER	
CHU, CHRIS C	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 12/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/933,492	HEMBREE ET AL.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE f this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *52 - 66 and 70 - 77* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *52 - 66 and 70 - 77* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on September 25, 2003 has been received and entered in the case.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 52 - 54, 60 – 62 and 70 – 76 are rejected under 35 U.S.C. 102(b) as being anticipated by Farnworth '911.

Regarding claims 52 and 53, Farnworth discloses in Fig. 2h, column 4, lines 55 - 61 and column 5, lines 6 – 13 a semiconductor component comprising:

- a substrate (semiconductor wafer) comprising a plurality of semiconductor components (semiconductor dice) including a plurality of patterns of component contacts (1002);
- a plurality of conductors (1016) on the components in electrical communication with the component contacts configured to redistribute the patterns of the component

contacts into selected patterns and to either repair, reconfigure, or electrically isolate selected components; and

- a plurality of terminal contacts (1032) on the components in the selected patterns in electrical communication with the conductors.

Regarding claim 54, Farnworth discloses in Fig. 2h and column 4, line 37 – 42 the conductors (1016) being contained in a metal redistribution layer.

Regarding claim 60, Farnworth discloses in Fig. 2h, column 4, lines 55 - 61 and column 5, lines 6 – 13 a semiconductor component (semiconductor dice) comprising:

- a semiconductor die (1004) comprising a plurality of integrated circuits (100) and a plurality of component contacts (1002) in a pattern in electrical communication with the integrated circuits;
- a plurality of conductors (1016) on the die in electrical communication with the component contacts configured to redistribute the pattern of the component contacts into a selected pattern; and
- a plurality of terminal contacts (1032) on the die in the selected pattern in electrical communication with the conductors.

Since the conductor (1016) in Fig. 2h of Farnworth necessarily does not connect the component contact (1002) to at least some of the other component contacts (otherwise the device would not operate as intended), the conductor (1016) of Farnworth is configured to electrically isolate the component contact (1002) from the other component contact. Therefore, Farnworth discloses the following limitation "at least some of the conductors configured to electrically isolate selected component contacts".

Regarding claim 61, Farnworth discloses in Fig. 2h, column 1, lines 45 – 54 and column 5, line 35 the terminal contacts (1032) comprising balls or bumps in a grid array.

Regarding claim 62, Farnworth discloses in Fig. 2h and column 4, line 37 – 42 the conductors (1016) being contained in a metal redistribution layer.

Regarding claim 70, Farnworth discloses in Fig. 2h and column 5, lines 6 – 13 a semiconductor component comprising:

- a semiconductor die (1004) comprising a plurality of contacts (1002) in a first pattern and a plurality of integrated circuits (100) in electrical communication with the contacts;
- a plurality of terminal contacts (1032) on the die in a second pattern; and
- a metal redistribution layer (1016) on the die containing a plurality of conductors configured to redistribute the first pattern of the contacts to the second pattern of the terminal contacts, and to either repair, reconfigure, or electrically isolate selected integrated circuits.

Regarding claim 71, Farnworth discloses in Fig. 2h, column 1, lines 45 – 54 and column 5, line 35 the terminal contacts (1032) comprising balls or bumps and the second pattern comprising a grid array.

Regarding claim 72, Farnworth discloses in Fig. 2h, column 4, lines 1 – 2, and column 5, lines 6 - 13 the contacts (1002) comprising bond pads.

Regarding claim 73, Farnworth discloses in Fig. 2h the conductors (1016) fanning out from the first pattern to the second pattern.

Regarding claim 74, Farnworth discloses in Fig. 2h and column 4, lines 55 - 61 the component (semiconductor dice) being contained on a substrate (a semiconductor wafer).

Regarding claim 75, Farnworth discloses in Fig. 2h, column 4, lines 55 - 61 a protective layer (1018) on the conductors (1016) having a plurality of openings (1026) for the terminal contacts (1032).

Regarding claim 76, Farnworth discloses in Fig. 2h and column 5, lines 38 – 40 the components (semiconductor dice) comprising a semiconductor package.

4. Claims 56 - 59 are rejected under 35 U.S.C. 102(b) as being anticipated by Dasse et al. '273.

Regarding claim 56, Dasse et al. discloses in e.g., Fig. 2 and column 11, lines 36 - 47 a semiconductor component comprising:

- a substrate (20) comprising a plurality of tested components (e.g., the elements 24 - 32) comprising a plurality of component contacts (see Fig. 3) in a plurality of patterns;
- the components (e.g., the elements 22 and 24 - 32) including a plurality of good components (e.g., any one of the elements 22, 24 - 27 and 29 - 32) and a defective component (28);
- a plurality of conductors (e.g., 45) configured to redistribute the patterns of the component contacts into selected patterns, to provide electrical paths for the component contacts on the good components; and

- a plurality of terminal contacts (88 one of the elements 24 - 27 and 29 - 32) on the good components in the selected patterns in electrical communication with the conductors.

Since the element 45 of Dasse et al. is connected to a current limiting resistor 77 which limits the current flow to or from the defective die 28, the element 45 electrically isolates the component contacts on the defective component. Therefore, Dasse et al. discloses the following limitation "a plurality of conductors ... [to] electrically isolate, the component contacts on the defective component".

Regarding claim 57, Dasse et al. discloses in e.g., Fig. 2 and column 4, line 7 the conductors (e.g., 45) being contained in a metal redistribution layer.

Regarding claim 58, Dasse et al. discloses in e.g., Fig. 14 the conductors being configured to electrically connect a plurality of good components in a cluster (514).

Regarding claim 59, Dasse et al. discloses in e.g., Fig. 2 the substrate (20) comprising a semiconductor wafer, and the components (22) comprising semiconductor dice or semiconductor packages.

5. Claims 63 - 66 are rejected under 35 U.S.C. 102(a)/102(b) as being anticipated by Cram '575.

Regarding claim 63, Cram discloses in Figs. 2A ~ 2C, column 1, lines 58 – 62 and column 2, lines 43 ~ 53 a test board for testing semiconductor components (12) on a substrate including a plurality of good components (12F) and at least one defective component (12NF), each component having a plurality of component contacts (16), the test board comprising:

- a plurality of first test sites (area for the 12F) on the test board (at the burn-in board under the wafer 10) comprising a plurality of contacts configured to electrically engage the component contacts (16) on the good components (12F) on the substrate (10); and
- a plurality of second test sites (area for the 12NF) on the test board configured to electrically isolate the defective component.

Regarding claim 64, Cram discloses in column 2, lines 43 ~ 53 the test board including a patterned metal layer (14 and air between 14s) containing a plurality of conductors (14) in electrical communication with the first test sites.

Regarding claim 65, Cram discloses in column 1, lines 58 – 62 and column 2, lines 43 ~ 53 the test board being configured to perform a burn-in test and the second test sites being configured to electrically isolate the defective component during the burn-in test.

Regarding claim 66, Cram discloses in Figs. 2A ~ 2C and column 1, lines 63 ~ 67 the substrate (10) comprising a semiconductor wafer, and the components (12) comprising dice or packages.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 55 is rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth in view of Dasse et al. '273.

Regarding claim 55, Farnworth does not disclose the conductors being configured to electrically connect multiple components in a cluster that excludes at least one defective component. Since the cluster (514) in e.g., Fig. 14 and Fig. 15 of Dasse et al. does not include any defective component, hence Dasse et al. teaches conductors (520) being configured to electrically connect multiple components (integrated circuit die) in a cluster (514) that excludes at least one defective component. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Farnworth by using the conductors as taught by Dasse et al. The ordinary artisan would have been motivated to modify Farnworth in the manner described above for at least the purpose of coupling to the integrated circuits in the cluster (column 25, lines 23 ~ 27).

8. Claim 77 is rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth in view of Franklin et al. '324.

Regarding claim 77, Farnworth discloses the claimed invention except for the conductors being configured to repair the at least one defective integrated circuits. However, Franklin et al. teaches in column 3, lines 13 – 27 conductors (metal strap repair line) being configured to repair the at least one defective integrated circuits. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Farnworth by using the conductors as taught by Franklin et al. The ordinary artisan would have been motivated to

modify Farnworth in the manner described above for at least the purpose of providing a fault free electronic package (column 1, lines 28 - 31).

Response to Arguments

9. Applicant's arguments with respect to claims 52 ~ 66 and 70 ~ 77 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7382.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
12/29/03 10:11:45 AM

BRADLEY BAUMEISTER
PRIMARY EXAMINER